Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application. In this response, claims 48, 49, 51-53 and 71 have been cancelled and claim 50 has been amended.

Claims 1–33 (canceled)

Claim 34 (previously presented) A test circuit for testing an integrated circuit on a wafer, the test circuit formed on the wafer with the integrated circuit, the test circuit comprising:

a) a base ring oscillator circuit;

b) a plurality of sub-circuits coupled to the base ring oscillator circuit; and

c) a control circuit to selectively couple the sub-circuits to the base ring oscillator circuit to produce different versions of a variable ring oscillator circuit associated with a selected sub-circuit,

and wherein the test circuit conducts a separate test of the integrated circuit for at least one of the versions of the variable ring oscillator circuit.

Claim 35 (original) The test circuit of claim 34 wherein each test conducted by the test circuit is a parametric test.

Claim 36 (previously presented) The test circuit of claim 35 wherein the sub-circuits when coupled to the base ring oscillator circuit change the frequency of oscillation of the variable ring oscillator circuit.

Claim 37 (previously presented) The test circuit of claim 36 wherein at least one sub-circuit comprises a capacitive load to change the frequency of oscillation of the variable ring oscillator circuit.

Claim 38 (previously presented) The test circuit of claim 36 wherein at least one sub-circuit comprises a capacitive load and a resistive load to change the frequency of oscillation of the variable ring oscillator circuit.

Claim 39 (previously presented) The test circuit of claim 38 wherein at least one sub-circuit comprises a delay element to change the frequency of oscillation of the variable ring oscillator circuit.

Claim 40 (original) The test circuit of claim 37 wherein the capacitive load comprises at least one capacitor.

Claim 41 (original) The test circuit of claim 38 wherein the capacitive load comprises at least one capacitor and the resistive load comprises at least one resistor.

Claim 42 (original) The test circuit of claim 39 wherein the delay element comprises at least one inverter.

Claim 43 (original) The test circuit of claim 42 wherein each inverter is a standard CMOS inverter.

Claim 44 (previously presented) The test circuit of claim 34 wherein the control circuit comprises a sequencer to selectively couple the sub-circuits to the variable ring oscillator circuit to produce a series of test states.

Claim 45 (original) The test circuit of claim 34 wherein the test circuit is formed on the wafer with at least two metallization layers of the integrated circuit.

Claim 46 (original) The apparatus of claim 34 wherein the test circuit is formed on the wafer with at least one metallization layer and one polysilicon layer of the integrated circuit.

Claim 47 (previously presented) The test circuit of claim 34 wherein the test circuit produces a test result signal that is the output of the variable ring oscillator circuit

Claims 48 and 49 (cancelled)

Claim 50 (currently amended) The apparatus of claim [[48]]44, wherein the control circuit further comprises a ring oscillator adapted to provide a first clock signal, and a divider coupled to the ring oscillator and the sequencer and adapted to provide a second clock signal, wherein the second clock signal is provided to the sequencer so that the sequencer can provide a series of test state signals to the variable ring oscillator circuit and plurality of sub-circuits.

Claims 51–53 (cancelled)

Claim 54 (original) The test circuit of claim 34 wherein the test circuit is formed adjacent to a die containing the integrated circuit.

Claim 55 (original) The test circuit of claim 34 wherein the test circuit is formed on a die that contains the integrated circuit.

Claim 56 (original) The test circuit of claim 34 wherein the test circuit is formed on a large percentage of dies on the wafer.

Claim 57 (original) The test circuit of claim 34 wherein the test circuit is formed on dies near the edge of the wafer.

Claims 58–72 (canceled)